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INVESTIGATION OF RADIATION-HARDENED CHARGE-COUPLED DEVICES.(U)
JAN 80 L R ROCKETT F19628-77-C-0247
UNCLASSIFIED RADC-TR-79-347 NL

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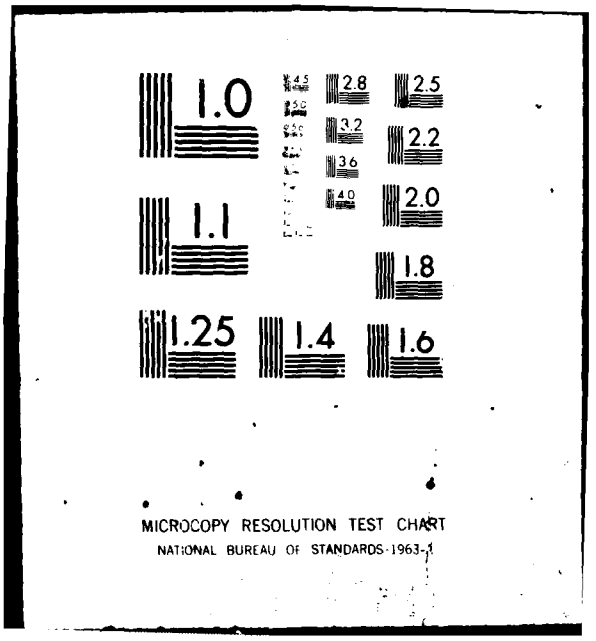
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TABLE 2. NTTC - P1HE RESULTS (NO BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(A)$	ε	V_ε
PRE	0	0	0	0
10^5	-0.3	+0.3	-2	-0.6
10^6	-0.1	+2.5	-1.04	-2.6
$5x10^6$	+0.3	+5.1	-0.94	-4.8

$\Delta V_T(M)$ - measured threshold voltage shift
$\Delta V_T(A)$ - actual threshold voltage shift

TABLE 3. NTTC - P2E RESULTS (NO BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(A)$	ε	V_ε
PRE	0	0	0	0
10^5	+0.3	-0.1	4	0.4
10^6	+1.2	+1.0	0.2	0.2
$5x10^6$	+2.1	+2.5	-0.16	-0.4

TABLE 4. NTTC - P2HE RESULTS (NO BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(A)$	ε	V_ε
PRE	0	0	0	0
10^5	+0.2	-1.0	1.2	1.2
10^6	+1.0	+0.3	2.33	0.7
$5x10^6$	+2.5	+2.5	~0	~0

The four versions of NTTCs were also irradiated with +10-V bias applied to the gates of the MOSFETs. The results of these tests are now presented.

The results of the standard and highly enhanced poly-1 NTTCs are given in Tables 5 and 6, respectively. The results of the standard and highly enhanced poly-2 NTTCs are given in Tables 7 and 8, respectively. Again, the circuits operated with large tracking errors.

TABLE 5. NTTC - P1E RESULTS (+10-V BIAS)

DOSE	ΔV_T(M)	ΔV_T(A)	ε	V_ε
PRE	0	0	0	0
10^4	-0.5	-0.5	~0	~0
$5x10^4$	-1.0	-2.7	0.63	1.7
10^5	-1.1	-2.1	0.48	1.0
$5x10^5$	-0.9	-0.7	-0.29	-0.2

TABLE 6. NTTC - P1HE RESULTS (+10-V BIAS)

DOSE	ΔV_T(M)	ΔV_T(A)	ε	V_ε
PRE	0	0	0	0
10^4	-0.3	-0.6	0.5	0.3
$5x10^4$	-0.8	-2.4	0.67	1.6
10^5	-1.2	-3.0	0.6	1.8
$5x10^5$	+0.8	-1.7	1.47	2.5

TABLE 7. NTTC - P2E RESULTS (+10-V BIAS)

DOSE	ΔV_T(M)	ΔV_T(A)	ε	V_ε
PRE	0	0	0	0
10^4	-0.1	-0.15	0.33	0.05
$5x10^4$	+0.15	-0.4	1.38	0.55
10^5	+0.3	-0.2	2.5	0.5
$5x10^5$	+0.6	+0.9	-0.33	-0.3

TABLE 8. NTTC - P2HE RESULTS (+10-V BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(A)$	ε	V_ε
PRE	0	0	0	0
10^4	-0.15	-0.1	-0.5	-0.05
$5x10^4$	+0.2	-0.6	1.33	0.8
10^5	+0.4	-0.4	2.0	0.8
$5x10^5$	+0.8	+0.3	1.67	0.5

b. PMOS Circuits

The TC1238 PMOS threshold tracking circuits (PTTC) were irradiated with and without -10-V bias applied to the transistor gates. (The p-channel threshold tracking circuits on TC1238 included designs that have standard poly-1 sensing devices with the remaining transistors being either depletion-type or enhancement-type devices.)

For the PTTCs that include depletion-type MOSFETs, their operation is analogous to the operation described for the NTTCs of the previous subsection. However, for the all-enhancement-type PTTCs, all transistors operate in the saturation region. For the all-enhancement PTTCs, the output of the source-follower stage varies with the absolute value of threshold voltage shifts with a slope approaching unity. The inverter stage output characteristic, however, is theoretically invariant to threshold shifts.

The results of the PTTC that have an enhancement-type poly-1 sensing device, with the other devices depletion-type irradiated with and without bias, are given in Tables 9 and 10, respectively. The results of the all-enhancement-type design of the poly-1 PTTCs irradiated with and without bias are given in Tables 11 and 12, respectively.

3. Automatic Input Biasing Circuit

The performance of the automatic input biasing (AIB) circuit after exposure to ionizing radiation was evaluated by determining the shape and position of its output characteristic specifically concentrating on the location of the dc operating point. Figures 42 and 43 show the experimental curves of two of

TABLE 9. PTTC - P1E RESULTS (-10-V BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(A)$	ε	V_ε
PRE	0	0	0	0
10^5	-0.8	-0.9	0.11	0.1
10^6	-0.6	-2.3	0.74	1.7

TABLE 10. PTTC - P1E RESULTS (NO BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(A)$	ε	V_ε
PRE	0	0	0	0
10^5	-0.7	-1.2	0.42	0.5
10^6	-1.0	-3.0	0.667	2.0

TABLE 11. PTTC - P1E (ALL-ENHANCEMENT) RESULTS (-10-V BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(A)$	ε	V_ε
PRE	0	0	0	0
10^5	-0.6	-0.8	0.25	0.2
10^6	-1.4	-2.3	0.39	0.9
$5x10^6$	-2.5	-4.0	0.38	1.5

TABLE 12. PTTC - P1E (ALL-ENHANCEMENT) (NO BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(A)$	ε	V_ε
PRE	0	0	0	0
10^5	-1.8	-1.2	-0.5	-0.6
10^6	-3.4	-3.0	-0.13	-0.4

the samples tested. Selecting the midrange point of the preirradiation curves of the devices as the dc operating point of the circuit it is apparent that by 10^6 rads (Si) the operating point is pinned at the low-end saturation region of the curve. This would provide no response by the circuit to small

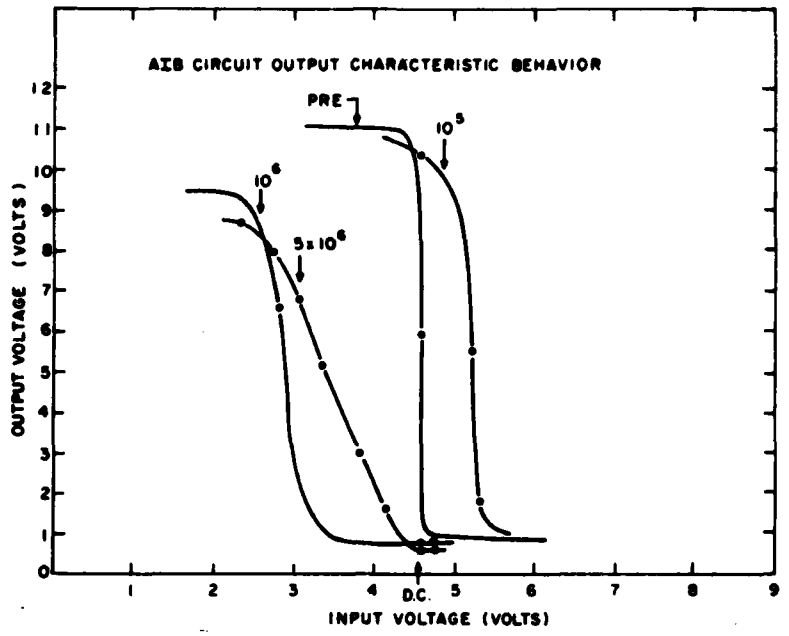

Figure 42. Output characteristics of automatic input biasing circuit -1 at radiation dose levels.

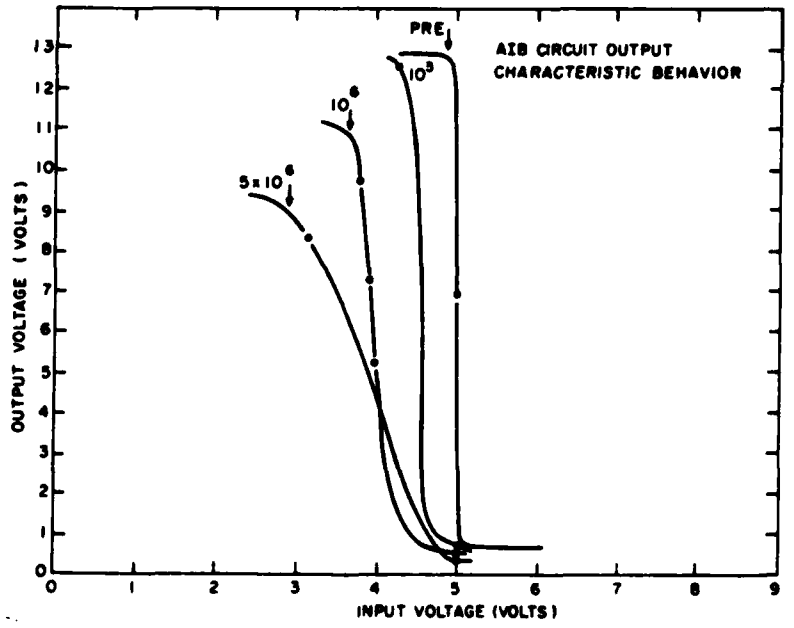

Figure 43. Output characteristics of automatic input biasing circuit -2 at radiation dose levels.

changes in charge on the integrating capacitor and, thus, the operation of the automatic input biasing fails. Note that radiation generally caused a large negative shift of the output characteristic and a reduction in the differential gain of this circuit.

The combined operation of the automatic input biasing circuit and the S-1 strobe-level circuit to improve the radiation tolerance of the BCCD input section was unachievable due to the failure of the AIB circuit to maintain operational stability with radiation.

4. Automatic Output Biasing Circuit

The behavior of the output characteristic of the differential comparator with radiation for two values of applied signal voltage (V_{IN}) is shown in Figs. 44 and 45. Note that as the reference voltage (V_{Ref}) approached the value of V_{IN}, the curves converged, as desired, though there was some reduction in differential gain for the range of radiation dose levels tested. However, when evaluating the complete automatic output-biasing (AOB) circuit, the best case results indicated that the circuit experienced severe overall gain loss with radiation. At 10^5 rads (Si) the AOB circuit gain had been reduced by 30 to 40% of its preirradiation value and by 10^6 rads (Si) the gain loss percentages were typically 65 to 80%. The gain unstability of this circuit with radiation is unacceptably high.

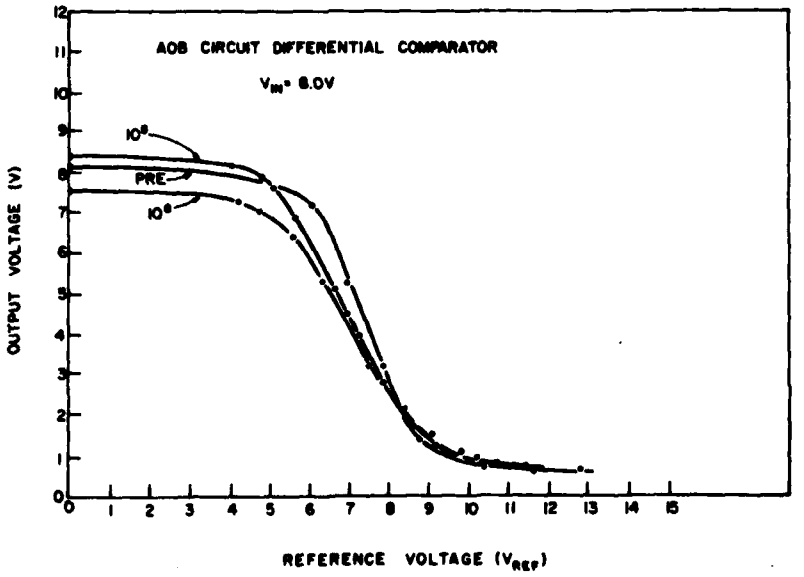

Figure 44. Output characteristic of differential comparator of automatic output biasing circuit at radiation dose levels with V_{IN} = 8.0 V.

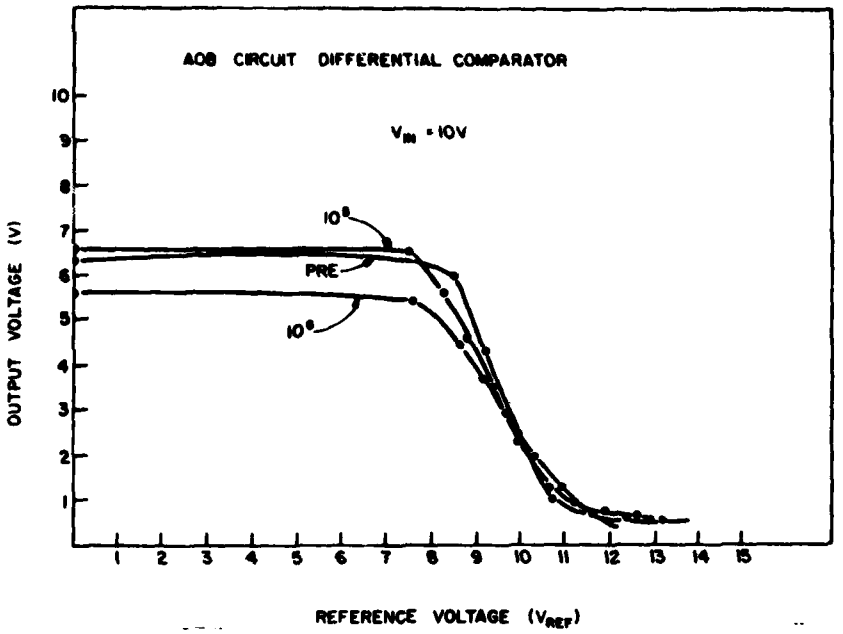

Figure 45. Output characteristics of differential comparator of automatic output biasing circuit at radiation dose levels with V_{IN} = 10.0 V.

C. DISCUSSION OF EXPERIMENTAL RESULTS

The TC1238 buried-channel CCD registers experienced large negative shifts in pin voltage with increasing radiation dose. The magnitude of these shifts was uncharacteristic of good radiation-hardened channel oxides [9,10]. The shifts made readjustment of the applied voltage levels necessary for cumulative radiation dose levels above 10^6 rads (Si) to prevent the signal charge from interacting with the interface states.

The signal-charge density of the BCCD registers did not suffer with increasing radiation dose levels. The registers still propagated better than 80% of their preirradiation signal-charge density for dose levels up to 10^6 rads (Si). This was a result of the nearly equal shift in pin voltage for the channel oxides under both gate levels for these devices irradiated without

9. C. P. Chang, "Radiation-Hardened Surface Channel CCDs," IEEE Trans. Nucl. Sci. NS-23, 1639 (1976).
10. C. P. Chang, "Radiation Effects in N-Buried-Channel CCDs Fabricated with a Hardened Process, "IEEE Nucl. Sci. NS-24, 1875 (1977).

bias over the dose range tested. Equal pin voltage shifts do little to alter the preirradiation potential well profiles of the registers and therefore there was no significant loss in signal capacity.

The initial dark-current densities of the BCCDs were relatively high. By 10^5 rads (Si) the dark-current density had increased by an order of magnitude and the increase approached two orders of magnitude by 10^7 rad (Si). The large increases in dark current were a consequence of the large density of interface states which acted as the generation centers for the surface component of dark-current generation.

The BCCD transfer inefficiency without fat zero increased by slightly less than a factor of 20 at 10^6 rads (Si) and by 10^7 rads (Si) ε had increased by an additional order of magnitude, that is a factor of $\sim$200. Although the signal charge in BCCD registers did not significantly interact with interface states, it was subject to bulk state trapping. At sufficiently high radiation dose levels, bulk trapping began to significantly affect the buried-channel transfer efficiency due to an increased density of bulk states.

The density of interface states increased with radiation dose at a rapid rate. By 10^5 rads (Si) the interface state density had increased by a factor of approximately 50 rendering the surface-channel CCDs essentially inoperative. The amount of interface states created by radiation is strongly dependent on the fabrication process, specifically the conditions and procedures involved in channel oxidation. A N_2 anneal after channel oxidation at the temperature of oxidation has been shown to be effective in reducing the interface state density [11].

In addition to seriously degrading SCCD performance and being the major cause of increased dark current in BCCDs, the large interface state densities caused the threshold voltage of n-channel MOSFETs to shift positively with radiation and also caused significant reductions in transconductance. When irradiated with no applied bias, the NMOS transistors, standard and highly enhanced enhancement-mode types, experienced a slight negative shift at 10^5 rads (Si), but beyond this point the threshold shifted positively until a second-threshold shift reversal occurred at $\sim 10^7$ rads (Si). The transconductance of the enhancement-mode transistors fell at a faster rate compared to the g_m of depletion-mode devices.

11. C. P. Chang, "Radiation-Hardened N-Buried-Channel CCDs Using Backside Phosphorus Gettering," IEEE Trans. Nucl. Sci. NS-25, 1454 (1978).

Essentially no difference in the degree of radiation hardness was detected between the first and second channel oxides when the devices were irradiated without bias since the state of the occupied interface states dominated the effects of the fixed positive oxide charges at the radiation dose levels tested. However, when devices were irradiated with +10-V bias at lower dose ranges to maximize the effects of the fixed positive oxide charge, there was a difference in radiation hardness detected. The first channel oxide layer was found to be less hard since it was subjected to more high-temperature processing and, therefore, greater threshold shifts were experienced by first polysilicon MOSFETs. Both standard and highly enhanced enhancement-mode NMOS devices irradiated with bias experienced negative shifts until a threshold shift reversal occurred at $\sim 5 \times 10^4$ rads (Si) due to the increasing domination by interface state trapping. The g_m plots for these devices showed the point of sharp reduction occurred at $\sim 5 \times 10^4$ rads (Si) also. The g_m reduction in enhancement-mode devices again was proportionally greater than that in depletion-mode devices.

For p-channel MOSFETs, occupied interface states enhanced the negative shift of threshold voltage. Radiation with an applied -10-V bias lessened the effect of fixed positive oxide charge by causing it to form near the gate electrode, and thus, the negative shift of biased PMOS devices was smaller compared to unbiased samples. Again, the g_m reduction was proportionally greater in enhancement-mode devices, though the recorded differences were smaller than those noted for the NMOS transistors.

The NMOS threshold tracking circuits irradiated with and without +10-V bias produced unacceptably large output voltage errors. The calculated fractional error (ε) was generally positive, indicating that the actual circuit output voltage was greater than the desired (ideal) output voltage. The most probable cause of the poor performance of the n-channel threshold tracking circuits was the differential reductions in g_m caused by interface state-trapping for enhancement-mode and depletion-mode devices. For both poly-1 and poly-2 NTTCs the greater reduction in g_m for the enhancement-mode sensing devices caused the circuit output voltage to be higher than the desired level because of its more rapidly increasing channel resistence.

All-enhancement-mode NTTCs were tested by externally addressing only NMOS transistors of similar construction available on the test chip to form the circuit. The devices were irradiated with +10-V applied bias. The best-case results of these experiments are given in Tables 13 and 14. These circuits

TABLE 13. NTTC - P1E (ALL-ENHANCEMENT) RESULTS (+10-V BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(AT)$	ε	V_ε
PRE	0	0	0	0
10^4	-0.5	-0.55	0.09	0.05
$5x10^4$	-1.0	-1.1	0.09	0.1
10^5	-0.6	-0.6	~0	~0
$5x10^5$	+0.1	+0.1	~0	~0

TABLE 14. NTTC - P2E (ALL-ENHANCEMENT) RESULTS (+10-V BIAS)

DOSE	$\Delta V_T(M)$	$\Delta V_T(A)$	ε	V_ε
PRE	0	0	0	0
10^4	-0.1	-0.1	~0	~0
$5x10^4$	-0.3	-0.4	0.25	0.1
10^5	+0.3	+0.3	~0	~0
$5x10^5$	+0.5	+0.6	-0.17	-0.1

performed with high accuracy for negative and positive threshold shifts as a result of the matching of the g_m characteristics of the devices that form the circuit.

It is not clear if the designed NTTCs on TC1238 which consist of depletion-mode MOSFETs with a single-enhancement-mode sensing device would perform with their predicted high accuracy if the creation of interface states was less pronounced so that the variations of g_m would be minimal. In an effort to determine the circuits' ability to track shifts in threshold voltage without significant g_m reductions, an output voltage versus varying substrate voltage dc test was run on the TC1238 NTTCs. The test results, however, were inconclusive since the I-V characteristics of NMOS depletion-mode transistors whose source region is at a potential higher than its substrate operating in nonsaturation varies very little over a wide range of substrate voltage. This specifically refers to transistors Q_3 and Q_4 of the NTTC design (Fig. 6) where the variations of their operating state with radiation is essential to the performance of the circuit.

The PMOS threshold tracking circuits irradiated with and without -10-V bias produced large output voltage errors. The all-enhancement-type PTTCs

generally operated better than the PTTCs with depletion-mode devices tested. This, again, was attributed to the g_m matching present in the all-enhancement-mode design. With more design optimizations and process improvements the PMOS TTCs could prove to be equally as feasible an approach for the threshold tracking circuit when used to interface with n-channel BCCDs for two notable reasons. First, the p-channel TTC operates with a negative oxide field just like n-channel BCCDs, and this, conceptually, might provide better tracking performance. Second, since the PTTCs must be fabricated in an N-well in a p-type wafer, the circuit's substrate is isolated from the substrate of the BCCD which allows greater flexibility in establishing the operating dc level of the CCD clock waveforms provided by the PTTC output voltage. The disadvantages of using PTTCs are the need to form an N-well during IC fabrication and PTTCs have generally provided poorer preirradiation performance, but this could improve with more design work.

The predesign computer simulations of the automatic input biasing circuit predicted very good performance. However, these simulations were performed assuming negative threshold voltage shifts and negligible interface state-trapping effects. Successful performance characteristics of the TC1238 circuits were not obtained owing to the effects of the large density of interface states on threshold voltage shifts and channel resistance variations. The instability of the transfer characteristic of the feedback amplifier prevented any evaluation of the AIB/S-1 strobe-level circuit combination as a technique for improving the radiation tolerance of the BCCD input section.

The use of an automatic output biasing circuit was shown unacceptable as a technique for improving the radiation tolerance of CCDs due to rapid circuit gain degradation. The gain instability resulted from the effects that radiation-induced positive oxide charge and reduced g_m's have in shifting the operating points of the high-gain stages of circuit, which, in turn, significantly alters the initial circuit characteristics. The preferred means of detecting the charge signal in a CCD is the use of a single on-chip MOSFET which is connected in a source-follower configuration using a discrete resistor element. This simple output circuit arrangement has been shown to be relatively insensitive to the effects of ionizing radiation [12].

12. J. M. Killiany, "Radiation Effect on Silicon Charge-Coupled Devices," IEEE Trans. on Comp., Hybrids, and Mfg. Tech. CHMT-1, 4, 353 (1978).

SECTION V

SUMMARY AND CONCLUSIONS

In this study, a test chip was specifically designed and fabricated to investigate techniques for improving the performance of CCDs in a nuclear radiation environment. The program focused on improving the radiation tolerance of 128-stage four-phase double-polysilicon n-buried-channel CCDs by using several specific circuit techniques to compensate for the harmful effects of ionizing radiation. The principal circuits included on the chip with the BCCD were automatic input and output biasing circuits and threshold tracking circuits. A n-surface-channel CCD was also included on chip to use as a test vehicle to evaluate the surface effects caused by radiation. The test chip was fabricated according to a low-temperature NMOS-CCD process which provided radiation-hard pyrogenically-grown (925°C) channel oxides of nearly-equal thickness under both the first and second levels of N^+-polysilicon gate electrodes. The devices were tested at various dose levels of high-energy (1 MeV) electron radiation.

The buried-channel CCDs experienced uncharacteristically large negative pin voltage shifts with radiation. The magnitude of the shifts were nearly equal under both gate levels and consequently there was no tendency to seriously degrade the signal-charge density of the devices. The dark-current densities of the BCCD registers rapidly increased by nearly two orders of magnitude and the BCCD transfer inefficiency was about a factor of 100 its initial value at 10^7 rads (Si). Large increases in the interface state density represented the major cause of the high levels of measured dark current, and increased bulk-state trapping caused the degradation in transfer efficiency.

The large interface state densities also adversely affected the operation of the on-chip peripheral circuits by severely altering the I-V characteristics of the MOSFET circuit components. There was generally a twofold effect of the interface states on the circuit components. First, above 10^5 rads (Si), the threshold voltage of the MOS transistors shifted positively with radiation, and second, electron-scattering greatly reduced the transconductances of the transistors. These effects severely affected the operation of the automatic input biasing circuits by causing the transfer characteristics of its feedback amplifier to be highly unstable with radiation. The automatic output biasing circuit suffered large gain degradation with radiation rendering it an impractical circuit technique for CCD radiation-hardening. The operation of the principal

NMOS and PMOS threshold tracking circuits produced unacceptably large output voltage errors with radiation. These TTCs were adversely affected by the variance in the differential transconductance of the enhancement-mode and depletion-mode transistors in the circuit design. However, TTCs consisting of all-enhancement-mode transistors operated with high accuracy. This provides the basis to set the following specific design guidelines for threshold tracking circuits.

(1) With the possible exception of depletion-mode MOSFETs for the voltage-divider stage, if one is desired, all MOSFETs of the TTC design should be enhancement-mode devices to avoid g_m matching errors.

(2) If needed, a threshold adjustment ion-implantation should be used to provide high preirradiation threshold voltages to ensure accurate circuit operation over an extended radiation dose range.

(3) The design of the source-follower stage is most critical in determining the accuracy of the circuit operation and, as such, maximizing the K_3/K_4 ratio is most important.

(4) All other TTC design specifications, described earlier in this report and repeated here for completeness, must be satisfied.

$$K_3 >> K_4$$
$$K_5 = K_6$$
$$t_{ox_3} = t_{ox_5}$$
$$t_{ox_6} = \text{specified CCD-gate oxide thickness}$$

Though the enhanced density of interface states was a major source of problems in this investigation, it has been shown that, when using low-temperature pyrogenically-grown channel oxides, a N_2 anneal at the oxide growth temperature is useful in reducing the interface state density [10].

The overall program objective of determining the optimum techniques for improving the radiation tolerance of CCDs was partially successful. The radiation hardness of the pyrogenic oxide layers did not achieve the expected high levels, as evidenced by the magnitude of the threshold voltage shifts and

the large density of interface states. In spite of this, the BCCDs operated efficiently through 10^6 rads (Si) of cumulative radiation dose. Highly accurate threshold tracking-circuit operation was obtained from specially constructed versions of NMOS TTCs which led to certain TTC design guidelines being formed. TTCs that are designed to conform to these guidelines represent a workable technique of improving the radiation tolerance of CCDs. The automatic output biasing circuit was determined to be an impractical technique for improved CCD radiation hardness, and a full evaluation of the automatic input biasing circuit was unobtainable due to circuit instability. Further studies that involve the development of a truly radiation-hard low-temperature NMOS-CCD technology and the evaluation of circuit techniques which incorporate specific design and process improvements are recommended.

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